REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-18 are pending. Claims 1-18 stand rejected.

Claims 1, 2, 6, 7, 8, 12, 13, 14, and 18 have been amended. Claims 19, 20, and 21 have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicant submits that the amendments do not add new matter.

Rejections Under 35 U.S.C. § 112

The Examiner has rejected claims 2, 8 and 14 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner has stated that

> Claims 2, 8 and 14 recite the limitation "the bus" in line 1. There is insufficient antecedent basis for this limitation in the claims.

(p. 2, Office Action 7/8/03)

In response, applicant has amended claims 1, 2, 7, 8, 13 and 14, to provide the proper antecedent basis for the limitation.

Rejections Under 35 U.S.C. 102(b)

Claims 1, 3-7, 9-13 and 15-18 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,812,562, of Baeg ("Baeg"). The Examiner stated that

As per claim 1, Baeg discloses the claimed invention including a method comprising:
ceasing bus access (all input signals are blocked when bus is in idle state; col. 5, line 37), in a configurable system on a chip (MSP), upon the occurrence of a specified event (e.g. issuing of clock stop request; see col. 4, lines 32 bridging col. 5, lines 1-40); allowing completion of all pending bus transactions (taught by Baeg as MSP will complete operation of the instructions in its instruction queue and then return to the idle state; col. 4, lines 60-65); stopping the system clock (all system clocks be stopped; col. 5, lines 21-40) such that the state of the hardware is held static (internal registers are in known state; col. 4, lines 35 and col. 5, lines 21-40); and accessing the static state of the hardware (scan internal registers) through a debug port (JTAG port 111) [see col. 5, lines 21-40; col. 3, lines 5-8].

(p. 3, Office Action 7/8/03)

Applicant respectfully submits that claim 1, as amended, is not anticipated by Baeg. Claim 1 includes the following limitations.

A method comprising:
recognizing an occurrence of a user-specified event;
generating a signal to cease bus access, in a configurable system on a chip, upon the occurrence of the user-specified event, the configurable system on a chip integrating at least a central processing unit, an internal system bus, and a configurable logic;
allowing completion of all pending bus transactions;
stopping the system clock such that the state of the hardware is held static; and
accessing the static state of the hardware through a debug port.

(Amended claim 1) (Emphasis added)

Baeg does not teach recognizing an occurrence of a user-specified event and ceasing bus access upon such occurrence. The Examiner cites the "issuing of clock stop request" as an example of such a user-specified event. However, as claimed, ceasing bus access is not the event, but is done in response to the event. Applicant has amended the claims to clarify this distinction. As claimed, the invention recognizes the occurrence of a user-specified event and generates a signal to cease bus access. Baeg does not disclose this limitation.

Applicant also respectfully submits that Baeg does not disclose a configurable system on a chip (CSOC) as described in the specification. The Examiner has equated the Multimedia Signal Processor (MSP™) of Baeg with the CSOC as claimed. The MSP does not integrate a CPU, a system bus, and configurable logic on a single chip (See U. S. Patent 6,192,073 to Reader et al., Figure 2 and col. 4, lines 18 - 33). In contrast, the CSOC as claimed, and as described in the specification, integrates at least a CPU, a system bus, and configurable logic. Applicant has amended the claims to clarify this distinction. The MSP described in Baeg can not be equated with the CSOC as claimed.

For these reasons, applicant respectfully submits that claim 1, as amended, is not anticipated by Baeg. Given that claims 3 – 6 depend, directly or indirectly, from claim 1, applicant respectfully submits that claims 3 – 6 are, likewise, not anticipated by Baeg. Moreover, given that claims 7 and 13 contain the limitations of "recognizing the occurrence of a user-specified event and generating a signal to cease bus access", applicant respectfully submits that claims 7 and 13 are not anticipated by Baeg for the reasons discussed above. Further, given that claims 9 – 12 and 15 - 18, depend, directly or indirectly, from claims 7 and 13, respectively, applicant respectfully submits that claims 9 - 12 and 15 – 18, are, likewise, not anticipated by Baeg.

Rejections Under 35 U.S.C. § 103(a)

Claims 2, 8 and 14 stand rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,812,562 of Baeg ("Baeg") in view of U.S. Patent No. 5,479,635 of Kametani ("Kametani").

The Examiner has rejected claims 2, 8 and 14 under 35 U.S.C. § 103 as being unpatentable over Baeg in view of Kametani. The Examiner has stated that

> As per claims 2, 8 and 14, Baeg disclosed the claimed invention including a bus except for a bus being a pipeline bus.
>
> Kametani, in his system for accessing memory device comprising of DRAMs, uses pipeline bus to achieve high-speed accessing. It would have been obvious to use a pipeline bus as taught by Kametani in the system of Baeg, since Baeg also employ a DRAM memory structure. Kametani taught that since pipeline bus access is an access system in which the address to be used in a given bus cycle is output in the preceding bus cycle (or processor cycle). The output is latched and then used in the actual bus cycle. Using pipeline bus for memory access makes it possible to take full advantage of the bus cycle time in carrying out access; thus allowing for high-speed accessing [see col. 12, lines 45-60].

(p. 7-8, Office Action 7/8/03)

> Kametani discloses
>
> The operation and effect of this embodiment will be better understood from FIG. 13(A) and 13(B). FIG. 13(B) shows the situation in the case of ordinary page access (in high-speed page mode) according to this invention. BS denotes the processor bus state and in this embodiment one bus cycle is equal to one processor cycle. Further, this embodiment relates to an application using a processor which conducts bus access using pipeline bus access. Pipeline bus access is an access system in which the address to be used in a given bus cycle is output in the preceding bus cycle (or processor cycle). The output address is latched and then used in the actual bus cycle. Use of this method makes it possible to take full advantage of the bus cycle time in carrying out access. With progressive reduction of processor machine cycle time, it will become increasingly difficult to secure adequate address access time when the address is output in the same...

(col. 12, lines 45-60)

Applicant respectfully submits, however, that claims 2, 8, and 14 are not obvious under 35 U.S.C. § 103 in view of Baeg and Kametani. It is respectfully submitted that Baeg does not teach or suggest a combination with Kametani and that Kametani does not teach or suggest a combination with Baeg. It would be impermissible hindsight based on applicant's own

disclosure to incorporate the memory device having DRAMs that are page-organized so as to reduce inter-page interference, disclosed in Kametani, into the integrated circuit providing emulation of VLSI chips of Baeg. Moreover, such a combination would still lack the limitations of "recognizing the occurrence of a user-specified event and generating a signal to cease bus access" as claimed.

For these reasons, applicant respectfully submits that claims 2, 8, and 14 are not rendered obvious by Baeg in view of Kametani.

Applicant further respectfully submits that new claims 19, 20, and 21 are not anticipated, nor rendered obvious, by Baeg or Kametani, alone or in combination. New claims 19, 20, and 21 include the limitation of the user-specified event comprising a sequence of events. Neither Baeg nor Kametani, alone or in combination, disclose this limitation.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 11/7/03 By: _____

Tom Van Zandt
Reg. No. 43,219

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(408) 720-8598